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semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	15

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DWPI	semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	2	L1
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EPAB	semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	0	L3
JPAB	semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	0	L4
PGPB	semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	0	L5
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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6057207 A

L1: Entry 1 of 2 File: DWPI May 2, 2000

DERWENT-ACC-NO: 2000-338611
DERWENT-WEEK: 200032

TITLE: Fabrication of a planarized insulating layer over a semiconductor structure involves using chemical-mechanical polishing processes to form openings and to planarize the layer

PAN:
TAIWAN SEMICONDUCTOR MFG CO

PAZZ:
TAIWAN SEMICONDUCTOR MFG CO

ABTX:
NOVELTY - A planarized first insulating layer is fabricated over a semiconductor structure by forming an etch layer over the non-conformal insulating layer; chemical-mechanical polishing (CMP) the etch barrier layer to form an opening; etching the insulating layer through the opening; and CMP the etch barrier and the insulating layers, the insulating layer fills the trenches between the raised portions.

ABTX:
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating a high density plasma chemical vapor deposition (HDPCVD) oxide filled shallow trench (40) isolation comprising: a) forming a first barrier layer (B) (24) composed of silicon nitride and has a thickness of 1,000-2,000 Angstrom over the pad oxide layer (A) (20); b) forming spaced trenches (3,000-6,000 Angstrom deep and greater than 0.2 mu m in width) in the semiconductor substrate (10) through (A) and (B) defining raised portions that are active areas in the semiconductor substrate with the wide raised portions (12A) having a width greater than 1.2 mu m; c) forming a first insulating layer (C) (5,000-8,000 Angstrom thick) composed of a non-conformal silicon oxide formed by a HDPCVD process filling the trench; d) forming an etch barrier layer (D) (200-500 Angstrom thick) composed of silicon nitride over (C); e) CMP the conformal (D) over the raised portions, forming a first opening to expose (C) over the wide raised portions; f) etching (C) through the first opening, exposing portions of (B); g) CMP (D) and (C) (filling the trenches between the raised portions)

to expose (B); h) removing (A) and (B) using an etch process, the top surface of (C) is higher by 300-700 Angstrom than the top surface of the raised portions.

ABTX:
USE - For planarizing an insulation layer over a semiconductor device.

ABTX:
ADVANTAGE - The method improves the planarization and reduces damage to the edges of the active areas.

ABTX:
Semiconductor substrate 10

ABTX:
Oxide filled shallow trench 40

TTX:
FABRICATE INSULATE LAYER SEMICONDUCTOR STRUCTURE CHEMICAL MECHANICAL POLISH PROCESS FORM OPEN LAYER

☐ 2. Document ID: US 6048775 A

L1: Entry 2 of 2 File: DWPI Apr 11, 2000

DERWENT-ACC-NO: 2000-328050
DERWENT-WEEK: 200028

TITLE: Fabrication of an integrated circuit by high-density plasma chemical deposition and chemical-mechanical polish processes

PAN:
VANGUARD INT SEMICONDUCTOR CORP

PAZZ:
VANGUARD INT SEMICONDUCTOR CORP

ABTX:
NOVELTY - Fabrication of an integrated circuit comprises providing a substrate (10), forming a non-conformal high density plasma chemical vapor deposition (HDPCVD) oxide layer (24), forming a second nitride layer (40), chemical-mechanical polishing, etching and removing the second nitride layer, and removing the first nitride layer.

ABTX:
DETAILED DESCRIPTION - Fabrication of an integrated circuit comprises: (a) providing a substrate having a surface and having formed a pad oxide layer and a first nitride layer; (b)

forming a non-conformal high density plasma chemical vapor deposition (HDPCVD) oxide layer extending over a surface of the first nitride layer adjacent to the trenches and filling the trenches; (c) forming a second nitride layer overlying the conformal HDPCVD oxide layer; (d) chemical-mechanical polishing the second nitride layer and the non-conformal HDPCVD oxide layer using the first and the second nitride layers as polish stops; (e) etching and removing the second nitride layer; and (f) removing the first nitride layer. The substrate has trenches comprised of narrow and wide trenches that define active areas. The first nitride is formed by a LPCVD process. The non-conformal HDPCVD layer deposited at a deposition to sputter ratio of 2.5:1-7:1 and the first nitride layer has DHF etch rate within 10% of the non-conformal HDPCVD oxide layer. The second nitride is formed by a plasma enhanced chemical vapor deposition process and has a chemical-mechanical polish ratio PE-Nitride:HDPCVD oxide of 2:1-3:1. The first and second nitride layers act as etch stops over more than 75% of the substrate area.

ABTX:
ADVANTAGE - The process prevents dishing in either the wide or narrow trenches. It uses an overlying nitride polish stop layer where the HPDCVD oxide had a Depth to Sputter ratio to form the nitride polish stop over the center of narrow trenches, thus acting as a polish stop in both the narrow and wide shallow trench isolation (STI) trenches.

ABTX:
DESCRIPTION OF DRAWING(S) - The figures show a cross-sectional view for illustrating a method of planarizing a non-conformal HPDCVD STI oxide layer.

ABTX:
Substrate 10

ABTX:
HDPCVD oxide layer 24

TTX:
FABRICATE INTEGRATE CIRCUIT HIGH DENSITY PLASMA CHEMICAL DEPOSIT CHEMICAL MECHANICAL POLISH PROCESS

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Terms	Documents
semiconductor and (substrate or wafer) and (trench or groove) and (HDPCVD or HDP or (high adj density adj plasma)) and (non adj conformal) and planar$	2

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☐ 1. Document ID: US 6270353 B1

L6: Entry 1 of 15 File: USPT Aug 7, 2001

US-PAT-NO: 6270353
DOCUMENT-IDENTIFIER: US 6270353 B1

TITLE: Low cost shallow trench isolation using non-conformal dielectric material

DATE-ISSUED: August 7, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Andrews; John W.	Wappinger Falls	NY	N/A	N/A
Hwang; Bao T.	Poughkeepsie	NY	N/A	N/A
Landis; Howard S.	Underhill	VT	N/A	N/A
Mei; Shaw-Ning	Poughkeepsie	NY	N/A	N/A
Tyler; James M.	Lagrangeville	NY	N/A	N/A
Vishnesky; Edward J.	Poughkeepsie	NY	N/A	N/A

US-CL-CURRENT: 434/424; 438/427

Full | Title | Citation | Front | Review | Classification | Date | Reference | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6232188 B1

L6: Entry 2 of 15 File: USPT May 15, 2001

US-PAT-NO: 6232188
DOCUMENT-IDENTIFIER: US 6232188 B1

TITLE: CMP-free disposable gate process

DATE-ISSUED: May 15, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Murtaza; Suhail	Dallas	TX	N/A	N/A
Chatterjee; Amitava	Plano	TX	N/A	N/A

US-CL-CURRENT: 438/300; 257/327

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 3. Document ID: US 6106678 A

L6: Entry 3 of 15 File: USPT Aug 22, 2000

US-PAT-NO: 6106678
DOCUMENT-IDENTIFIER: US 6106678 A

TITLE: Method of high density plasma CVD gap-filling

DATE-ISSUED: August 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shufflebotham; Paul Kevin	San Jose	CA	N/A	N/A
Weise; Mark	San Jose	CA	N/A	N/A

US-CL-CURRENT: 204/192.32; 204/192.3, 204/192.37, 204/298.09, 204/298.15, 427/574, 427/579

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6095084 A

L6: Entry 4 of 15 File: USPT Aug 1, 2000

US-PAT-NO: 6095084
DOCUMENT-IDENTIFIER: US 6095084 A

TITLE: High density plasma process chamber

DATE-ISSUED: August 1, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shamouilian; Shamouil	San Jose	CA	N/A	N/A
Kumar; Ananda H.	Milpitas	CA	N/A	N/A
Kholodenko; Arnold	San Francisco	CA	N/A	N/A
Grimard; Dennis S.	Ann Harbor	MI	N/A	N/A
Mohn; Jonathan D.	Saratoga	CA	N/A	N/A
Chafin; Michael G.	San Jose	CA	N/A	N/A
Collins; Kenneth S.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 118/723E; 156/345, 216/67, 361/234, 438/656, 438/710

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 5. Document ID: US 6095083 A

L6: Entry 5 of 15 File: USPT Aug 1, 2000

US-PAT-NO: 6095083
DOCUMENT-IDENTIFIER: US 6095083 A

TITLE: Vacuum processing chamber having multi-mode access

DATE-ISSUED: August 1, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rice; Michael	Pleasanton	CA	N/A	N/A
Askarinam; Eric	Sunnyvale	CA	N/A	N/A
Schneider; Gerhard	Cupertino	CA	N/A	N/A
Collins; Kenneth S.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 118/723I; 118/715, 118/724, 118/733, 156/345

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 6. Document ID: US 6077571 A

L6: Entry 6 of 15 File: USPT Jun 20, 2000

US-PAT-NO: 6077571
DOCUMENT-IDENTIFIER: US 6077571 A

TITLE: Conformal pure and doped aluminum coatings and a methodology and apparatus for their preparation

DATE-ISSUED: June 20, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kaloyeros; Alain E.	Voorheesville	NY	N/A	N/A
Faltermeier; Jonathan	Clifton Park	NY	N/A	N/A

US-CL-CURRENT: 427/576; 427/252, 427/253, 427/255.7, 427/376.7, 438/680, 438/681, 438/687, 438/688

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 7. Document ID: US 6074512 A

L6: Entry 7 of 15 File: USPT Jun 13, 2000

US-PAT-NO: 6074512
DOCUMENT-IDENTIFIER: US 6074512 A

TITLE: Inductively coupled RF plasma reactor having an overhead solenoidal antenna and modular confinement magnet liners

DATE-ISSUED: June 13, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Collins; Kenneth	San Jose	CA	N/A	N/A
Rice; Michael	Pleasanton	CA	N/A	N/A
Buchberger; Douglas	Pleasanton	CA	N/A	N/A
Roderick; Craig	San Jose	CA	N/A	N/A
Askarinam; Eric	Sunnyvale	CA	N/A	N/A
Schneider; Gerhard	Cupertino	CA	N/A	N/A
Trow; John	San Jose	CA	N/A	N/A
Tsui; Joshua	Santa Clara	CA	N/A	N/A
Grimard; Dennis	Ann Arbor	MI	N/A	N/A
Yin; Gerald	Cupertino	CA	N/A	N/A
Wu; Robert	Pleasanton	CA	N/A	N/A

US-CL-CURRENT: 156/345; 118/723AN, 118/723E, 118/723I, 118/723IR, 204/298.06, 204/298.15, 204/298.16, 204/298.31, 204/298.34, 204/298.37

Full | Title | Citation | Front | Review | Classification | Date | Reference | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6063233 A

L6: Entry 8 of 15 File: USPT May 16, 2000

US-PAT-NO: 6063233
DOCUMENT-IDENTIFIER: US 6063233 A

TITLE: Thermal control apparatus for inductively coupled RF plasma reactor having an overhead solenoidal antenna

DATE-ISSUED: May 16, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Collins; Kenneth	San Jose	CA	N/A	N/A
Rice; Michael	Pleasanton	CA	N/A	N/A
Askarinam; Eric	Sunnyvale	CA	N/A	N/A
Buchberger; Douglas	Tracy	CA	N/A	N/A
Roderick; Craig	San Jose	CA	N/A	N/A

US-CL-CURRENT: 156/345; 118/723AN, 118/723E, 118/723I, 118/723IR, 118/724, 204/298.09, 204/298.31, 204/298.34

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 9. Document ID: US 6057207 A

L6: Entry 9 of 15 File: USPT May 2, 2000

US-PAT-NO: 6057207
DOCUMENT-IDENTIFIER: US 6057207 A

TITLE: Shallow trench isolation process using chemical-mechanical polish with self-aligned nitride mask on HDP-oxide

DATE-ISSUED: May 2, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chung-Te	Tainan	N/A	N/A	TWX
Ho; Chin-Hsiun	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 438/424; 438/425, 438/427

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 10. Document ID: US 6057210 A

L6: Entry 10 of 15 File: USPT May 2, 2000

US-PAT-NO: 6057210
DOCUMENT-IDENTIFIER: US 6057210 A

TITLE: Method of making a shallow trench isolation for ULSI formation via in-direct CMP process

DATE-ISSUED: May 2, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yang; Fu-Liang	Tainan	N/A	N/A	TWX
Lin; Wei-Ray	Yi Lan	N/A	N/A	TWX
Kuo; Ming-Hong	Pintung	N/A	N/A	TWX

US-CL-CURRENT: 438/427; 148/DIG.50, 438/424, 438/435, 438/437

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 11. Document ID: US 6048775 A

L6: Entry 11 of 15 File: USPT Apr 11, 2000

US-PAT-NO: 6048775
DOCUMENT-IDENTIFIER: US 6048775 A

TITLE: Method to make shallow trench isolation structure by HDP-CVD and chemical mechanical polish processes

DATE-ISSUED: April 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yao; Liang-Gi	Taipei	N/A	N/A	TWX
Hsu; Stanley	Tainan	N/A	N/A	TWX
Chang; Randy	Hsinchu	N/A	N/A	TWX
Lin; Albert	Tainan	N/A	N/A	TWX

US-CL-CURRENT: 438/427; 438/424, 438/428, 438/438

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 12. Document ID: US 6001740 A

L6: Entry 12 of 15 File: USPT Dec 14, 1999

US-PAT-NO: 6001740
DOCUMENT-IDENTIFIER: US 6001740 A

TITLE: Planarization of a non-conformal device layer in semiconductor fabrication

DATE-ISSUED: December 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Varian; Kathryn H.	Hopewell Junction	NY	N/A	N/A
Tobben; Dirk	Fishkill	NY	N/A	N/A
Sendelbach; Matthew	Wappingers Falls	NY	N/A	N/A

US-CL-CURRENT: 438/692; 216/38, 438/719, 438/756

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 13. Document ID: US 5899736 A

L6: Entry 13 of 15 File: USPT May 4, 1999

US-PAT-NO: 5899736
DOCUMENT-IDENTIFIER: US 5899736 A

TITLE: Techniques for forming electrically blowable fuses on an integrated circuit

DATE-ISSUED: May 4, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Weigand; Peter	Unterhaching	N/A	N/A	DEX
Tobben; Dirk	Fishkill	NY	N/A	N/A

US-CL-CURRENT: 438/601; 438/467

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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☐ 14. Document ID: US 5880007 A

L6: Entry 14 of 15 File: USPT Mar 9, 1999

US-PAT-NO: 5880007
DOCUMENT-IDENTIFIER: US 5880007 A

TITLE: Planarization of a non-conformal device layer in semiconductor fabrication

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Varian; Kathryn H.	Hopewell Junction	NY	N/A	N/A
Tobben; Dirk	Fishkill	NY	N/A	N/A
Sendelbach; Matthew	Wappingers Falls	NY	N/A	N/A

US-CL-CURRENT: 438/427; 438/424

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

☐ 15. Document ID: US 5854126 A

L6: Entry 15 of 15 File: USPT Dec 29, 1998

US-PAT-NO: 5854126
DOCUMENT-IDENTIFIER: US 5854126 A

TITLE: Method for forming metallization in semiconductor devices with a self-planarizing material

DATE-ISSUED: December 29, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tobben; Dirk	Fishkill	NY	N/A	N/A
Spuler; Bruno	Wappingers Falls	NY	N/A	N/A
Gutsche; Martin	Poughkeepsie	NY	N/A	N/A
Weigand; Peter	Unterhaching	N/A	N/A	DEX

US-CL-CURRENT: 438/626; 438/631, 438/636, 438/669, 438/760

Full | Title | Citation | Front | Review | Classification | Date | Reference KWIC | Draw Desc | Image

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